REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-14, 16, 18, and 20-22 are pending in this application. Claims 15, 17, and 19 are canceled by the present response without prejudice. Claims 1-22 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent 4,481,573 to Fukunaga et al. (herein "Fukunaga").

Addressing the above-noted rejection based on Fukunaga, that rejection is traversed by the present response.

Initially, applicants note each of the independent claims is amended by the present response to clarify features recited therein. Independent claim 1 now recites at least first and second transfer means, and:

> wherein each of said first and second transfer means includes an independent respective first and second virtual address space each including virtual addresses, wherein the virtual addresses in the first virtual address space overlap with the virtual addresses in the second virtual address space[.]

The other independent claims are similarly amended.

According to such claimed features, and with reference to Figures 5 and 6 in the present specification as a non-limiting example, first and second transfer means, such as an instruction bus 71 and a data bus 72, are provided. Further, each of those first and second transfer means includes an independent respective first and second virtual address space, see instruction virtual address space 101 for the instruction bus 71 and data virtual address space 102 for the data bus 72. The virtual addresses in the first virtual address space 101 overlap with the virtual addresses in the second virtual address space 102.[1]

As also previously recited in the claims the virtual address space for each respective first and second transfer means is translated into a single physical address space.

[1] See also the discussion in the present specification at page 25, line 14 et seq.

The above-noted claimed features are believed to clearly distinguish over Fukunaga.

With respect to features of the transfer means and the independent virtual address spaces, which are now clarified in the claims, the outstanding Office Action cited Fukunaga at the Abstract, column 2, lines 56-58, and Figure 1.

In that respect applicants submit no disclosure in Fukunaga is directed to the claimed features. Fukunaga discloses a virtual storage data processing system having an address translation unit shared by a plurality of processors. In column 2, lines 56-58 Fukunaga states "[f]ourthly, in a highly pipelined controlled processor, a unit for accessing an instruction is separate from a unit for accessing an operand and they have cache memories of their own to attain high speed operation".

Such disclosures in Fukunaga are not directed to the claimed features. Specifically, Fukunaga does not disclose or suggest:

> wherein each of said first and second transfer means includes an independent respective first and second virtual address space each including virtual addresses, wherein the virtual addresses in the first virtual address space overlap with the virtual addresses in the second virtual address space.

Utilizing different units for accessing an instruction and for accessing an operand is not directed to such claim features, and does not even address similar features as in the claims in which virtual addresses and first and second address spaces for first and second transfer means overlap with each other.

Thereby, the claims as currently written are believed to clearly distinguish over Fukunaga.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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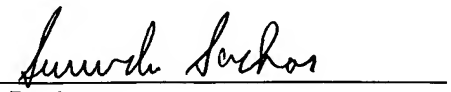

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